REMARKS

Claims 1 to 77 were pending in the application at the time of examination. The Examiner rejected Claims 1 to 77 under 35 U.S.C. 102(e) as anticipated by the Camporese et al reference (US 6,205,571).

Claims 1 to 77 remain in the application.

REJECTION OF CLAIMS 1 TO 77 UNDER 35 U.S.C.102(E) AND CAMPORESES

The Examiner rejected Claims 1 to 77 under 35 U.S.C. 102(e) as anticipated by the Camporese et al reference (US 6,205,571).

Applicants' Claim 1 recites the following, with emphasis added:

> A method of determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the method comprising:
>
> partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;
>
> simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, **said simulating including measuring clock arrival time and slope at each point where a clock element is connected**;
>
> simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets; and
>
> combining the plurality of simulations to form a complete clock net simulation.

Applicants' Claim 16 recites the following, with emphasis added:

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> An apparatus for determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the apparatus comprising:
>
> means for partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;
>
> means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, **said means for simulating including means for measuring clock arrival time and slope <u>at each point</u> where a clock element is connected**;
>
> means for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets; and
>
> means for combining the plurality of simulations to form a complete clock net simulation.

Applicants' Claim 31 recites the following, with emphasis added:

> An apparatus for determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the apparatus comprising:
>
> a partitioner for horizontally and vertically partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;
>
> at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, said local net simulator including **a clock monitor for measuring clock arrival time and slope <u>at each point</u> where a clock element is connected**;
>
> a global clock net simulator for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets; and

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a merging unit for combining the plurality of simulations to form a complete clock net simulation.

Applicants' Claim 43 recites the following, with emphasis added:

A computer-readable medium having stored thereon computer-executable instructions for performing a method of determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the method comprising:

partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, **said simulating including measuring clock arrival time and slope <u>at each point</u> where a clock element is connected;**

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets; and

combining the plurality of simulations to form a complete clock net simulation.

Applicants' Claim 58 recites the following, with emphasis added:

A method of determining and analyzing clock insertion delays for a microprocessor design having a grid-based clock distribution net, the method comprising:

partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, **said simulating including measuring clock arrival time and slope <u>at each point</u> where a clock element is connected;**

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simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form a complete clock net simulation; and

analyzing the complete clock net to predict the clock skew for a given data transfer path.

Applicants' Claim 63 recites the following, with emphasis added:

An apparatus for determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the apparatus comprising:

means for partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, **said simulating including measuring clock arrival time and slope <u>at each point</u> where a clock element is connected;**

means for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

means for combining the plurality of simulations to form a complete clock net simulation; and

means for analyzing the complete clock net to predict the clock skew for a given data transfer path.

Applicants' Claim 68 recites the following, with emphasis added:

An apparatus for determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the apparatus comprising:

a partitioner for horizontally and vertically partitioning the complete grid-based clock

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distribution net into a global clock net and a plurality of local clock nets;

at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, **said simulating including measuring clock arrival time and slope at each point where a clock element is connected;**

a global clock net simulator for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

a merging unit for combining the plurality of simulations to form a complete clock net simulation; and

an analyzer for analyzing the complete clock net to predict the clock skew for a given data transfer path.

Applicants' Claim 73 recites the following, with emphasis added:

A computer-readable medium having stored thereon computer-executable instructions for performing a method of determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the method comprising:

partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, **said simulating including measuring clock arrival time and slope at each point where a clock element is connected;**

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form a complete clock net simulation; and

analyzing the complete clock net to predict the clock skew for a given data transfer path.

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As shown above each of Applicants' independent Claims 1, 16, 31, 43, 58, 63, 68 and 73 includes the specific limitation that **said simulating includes measuring clock arrival time and slope at each point where a clock element is connected**, or words to that effect.

As Applicants have previously pointed out to the Examiner, **since Camporese focuses on approximation of various clock loads, all effects of the neighboring sectors are represented by the clustered grid loads (see ABSTRACT thereof). Thus, Camporese's simulation is only X-Y grid based (see FIGS. 9-10 thereof), and does not measure or observe the clock skew at specific points where clock elements are connected.** As Applicants have also pointed out, measuring at specific points is contrary to Camporese's clustering and smoothing of the clock loads. Consequently, Camporese actually teaches away from Applicants' invention as recited in Applicants' Claims 1, 16, 31, 43, 58, 63, 68 and 73.

In addition, Camporese does not mention "clock slope" at all or any use of this parameter. The Examiner states that, presumably to his belief, "it is well known in the art that delay times are based on the slope of input transitions". However, the Examiner fails to show where this is discussed in Camporese, or any other reference, and more importantly, where Camporese discloses, teaches or suggests **measuring clock arrival time and slope at each point where a clock element is connected.**

In light of the discussion above, Applicants' respectfully submit that the Camporese reference fails to disclose, teach or suggest **measuring clock arrival time and slope at each point where a clock element is connected,** as recited in each of Applicants' independent Claims 1, 16, 31, 43, 58, 63, 68 and 73 and therefore Applicants' independent Claims 1, 16, 31, 43, 58, 63, 68 and 73 are patentable over the Camporese reference for

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at least this reason. Consequently, Applicants respectfully request allowance of Claims 1, 16, 31, 43, 58, 63, 68 and 73.

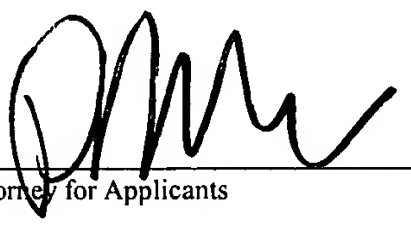
In addition, Claims 2-15 depend from Claim 1, Claims 17-30 depend from Claim 16, Claims 32-42 depend from Claim 31, Claims 44-57 depend from Claim 43, Claims 59-62 depend from Claim 58, Claims 64-67 depend from Claim 63, Claims 69-72 depend from Claim 68, and Claims 74-77 depend from Claim 73, and thus include the limitations of respective independent claims. Consequently, Applicants respectfully submit that Claims 2-15, 17-30, 32-42, 44-57, 59-62, 64-67, 69-72, and 74-77 are patentable over the Camporese et al reference for at least the reasons discussed above. Therefore Applicants respectfully request allowance of Claims 2-15, 17-30, 32-42, 44-57, 59-62, 64-67, 69-72, and 74-77 as well.

CONCLUSION

For the foregoing reasons, Applicants respectfully request allowance of all pending Claims 1 to 77. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants.

CERTIFICATE OF MAILING

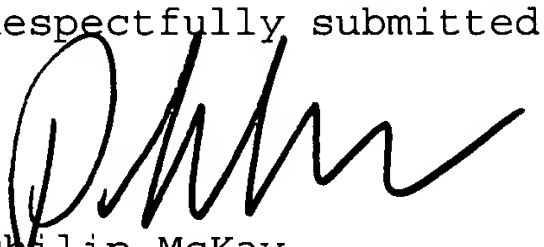
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 21, 2004.



Attorney for Applicants

December 21, 2004
Date of Signature

Respectfully submitted,



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